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| 10/033,155 | 10/25/2001 | Sailesh Kottapalli | 42P12494 | 7078 |

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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/033,155 | KOTTAPALLI ET AL. | |
| | Examiner | Art Unit | |
| | John P Trimmings | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-17 are presented for examination.

### *Information Disclosure Statement*

The examiner has considered the reference disclosed in the applicant's IDS of 10/25/2001.

### *Drawings*

1. New corrected drawings are required in this application because Figure 1 lacks a formal form. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

### *Specification*

*2.* The disclosure is objected to because of the following informalities: The SUMMARY OF THE INVENTION is missing. As provided in 37 CFR 1.77(b), the specification of a utility application should include the Summary. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not describe or specify the action taken in this claim, namely; "disabling the cache lines when the status bit indicates the defect".

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by McClure, U.S. Patent No. 5666482.

As per Claim 1:

McClure teaches an apparatus comprising: a processor (column 10 lines 22-23), coupled to a cache memory (column 10 lines 20-21); the cache memory with a plurality of cache lines (column 8 line 44), each cache line with at least one status bit to represent whether the cache line contains a defect (column 8 lines 59-61); and a logic to perform at least one test of the plurality of cache lines and to set the status bit for at least one of the plurality of cache lines (column 8 lines 53-61).

As per Claim 2:

McClure teaches the apparatus of claim 1 wherein the logic is a programmable built in self-test (PBIST) logic (column 10 lines 3-4).

As per Claim 5:

McClure teaches the apparatus of claim 1 wherein the status bit is stored in a register file cell (column 10 lines 1-2).

As per Claim 8:

McClure teaches the apparatus of claim 1 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache (column 10 lines 22-23 and column 2 lines 29-36).

6. Claims 14-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Phan, U.S. Patent No. 6634003.

As per Claim 14:

Phan teaches a method of configuring a cache memory with a plurality of cache lines (FIG.1 12) comprising: testing the plurality of cache lines (column 4 lines 25-38); setting a status bit for at least one cache line to indicate whether the cache line has a

defect as a result of the testing (column 6 lines 8-65). The examiner wishes to note that there is no support for "disabling the cache lines when the status bit indicates the defect" (see Phan Abstract) in the specification, and so this feature is moot.

As per Claim 15:

Phan teaches the method of claim 14 wherein the setting a status bit comprises storing the bit in either one of a six-transistor static random access memory cell, a register file cell, or a fuse (see register file cell in FIG.4).

As per Claim 16:

Phan teaches the method of claim 14 wherein the status bit is stored in either one of a six-transistor static random access memory cell, a register file cell, or a fuse (see register file cell in FIG.4).

As per Claim 17:

Phan teaches the method of claim 14 wherein the status bit is a read only bit during normal operation of the cache memory. The status bit (FIG.4) is activated only during test and initialization (column 6 lines 8-65), and therefore is read only in normal operation (column 4 lines 11-24).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482., and in view of Crouch et al., U.S. Patent No. 5592493. McClure teaches the apparatus of claim 1 wherein the logic is a plurality of scan chains (column 10 lines 1-2), but does not teach a test access port to accept automatic test pattern generation (ATPG) patterns. But in an analogous art, Crouch et al. tests a cache (column 7 lines 5-10) using a test access port (column 2 lines 5-13), using ATPG patterns (column 2 lines 51-65). It would have been obvious to modify the apparatus of

McClure by providing a TAP such as the one taught by Crouch et al. in order to utilize ATPG patterns. And Crouch et al., in column 1 lines 10-30, recites a need to efficiently test and to access components such as a cache by using this invention. One with ordinary skill in the art at the time of the invention, motivated by Crouch et al., would combine the references, and so the claim is rejected.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482., and in view of the applicant's admitted prior art. McClure teaches the apparatus of claim 1 wherein the status bit is stored in a six-transistor static random access memory cell (column 10 lines 5-6). The examiner notes that it is well known in the art that a non-volatile device is an SRAM device, and a six-transistor SRAM device is admitted prior art for an SRAM as admitted to by the applicant (Application, page 5 line 19).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482, in view of Aipperspach et al., U.S. Patent No. 6181614. McClure teaches the apparatus of claim 1 but does not specifically teach wherein the status bit is stored in a fuse. In analogous art, Aipperspach et al. does teach this feature in column 2 lines 21-22. It would have been obvious to modify the circuit of McClure to include permanently modifiable cells of a fusible type to make changes permanent. And in column 2 lines 1-20 the inventor describes the advantage of a self-repair system using persistent repair information. One with ordinary skill in the art at the time of the invention, motivated by Aipperspach et al., would combine the references, and so the claim is rejected.

10. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, U.S. Patent No. 5666482, in view of Phan, U.S. Patent No. 6634003.

As per Claim 9:

McClure teaches the apparatus of claim 1 but is not specific in teaching that the status bit is a read only bit during normal operation of the system. In an analogous art, Phan does teach this feature. The status bit (FIG.4) is activated only during test and initialization (column 6 lines 8-65), and therefore is read only in normal operation (column 4 lines 11-24). It would have been obvious to make the replacement circuits non-modifiable during normal operation as taught by Phan. And Phan, in column 1 lines 47-61 recites need to improve circuit speed by using the status bit instead of address compares for fault indication during normal operation of a cache. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Phan, would combine the references, and thus the claim is rejected.

As per Claim 9:

McClure teaches the apparatus of claim 2, and Phan teaches wherein the PBIST logic can set the status bit during initialization of the cache memory (column 6 lines 8-65). And in view of the obviousness and motivation already recited, the claim is rejected.

11. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edmondson et al., U.S. Patent No. 5680544, in view of Phan, U.S. Patent No. 6634003.

As per Claim 10:

Edmondson et al. teaches an article comprising: a storage medium having stored thereon instructions (see columns 7 and 8 for example), that, when executed by a computing platform (see Abstract), result in execution of testing a processor's cache memory with a plurality of cache lines (column 3 lines 40-52 and Abstract); generating a test pattern (column 3 line 51); stimulating the cache memory with the test pattern (column 3 lines 49-51), but does not teach writing to at least one status bit for each cache line to indicate whether the cache line contains a defect. In analogous art, Phan does teach this feature, where (see FIG.4) there is writing to at least one status bit for each cache line to indicate whether the cache line contains a defect (column 5 lines 28-56). And in view of the obviousness and motivation for Phan previously recited, the claim is rejected.

As per Claim 11:

The article of claim 10 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache is further taught by Edmondson et al. in column 13 lines 12-13. And in view of the same obviousness and motivation for Phan above, the claim is rejected.

As per Claim 12:

The article of claim 10 wherein the status bit is stored in either one of a six-transistor static random access memory cell, a register file cell, or a fuse. Phan, in FIG.4 shows a latch for storage, which in the art is a register file cell. It would have been obvious to one of ordinary skill to equate a latch to a register as is taught by

Phan, and to modify the name of the Edmondson et al. circuit thusly. And in view of the motivation for Phan above, the claim is rejected.

As per Claim 13:

The article of claim 10 is limited wherein Phan teaches the status bit as being a read only bit during normal operation of the cache memory. The status bit (Phan FIG.4) is activated only during test and initialization (Phan column 6 lines 8-65), and therefore is read only in normal operation (Phan column 4 lines 11-24). And in view of the obviousness and motivation for Phan above, the claim is rejected.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

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